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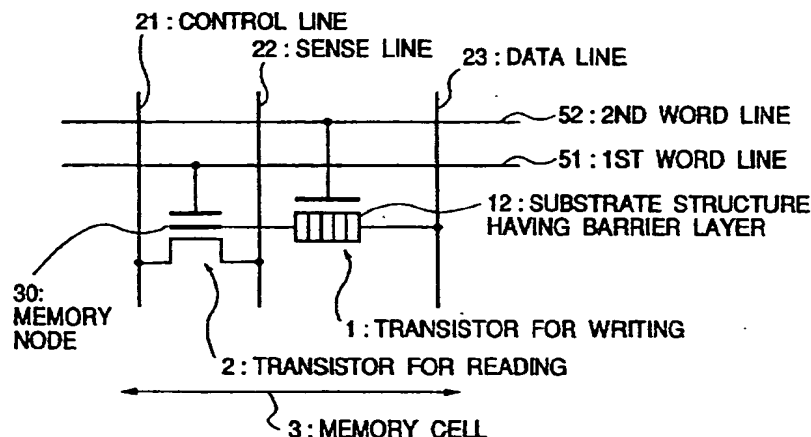
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(54) Semiconductor memory device and manufacturing method thereof

(57) A high speed/large capacity DRAM (Dynamic Random Access Memory) is generally refreshed each 0.1 sec because it loses information stored therein due to a leakage current. The DRAM also loses information stored therein upon cutoff of a power source. Meanwhile, a nonvolatile ROM (Read-only Memory) cannot be configured as a high speed/large capacity memory.

A semiconductor memory device of the present invention realizes nonvolatile characteristic by shielding a drain functioning as a memory node from a leakage current by a tunnel insulator, and also realizes stable and high speed operation by adding a transistor for reading to a memory cell.

FIG. 2



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Place of search BERLIN		Date of completion of the search 26 May 1999	Examiner Polesello, P
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A semiconductor memory device of the present invention realizes nonvolatile characteristic by shielding a drain functioning as a memory node from a leakage current by a tunnel insulator, and also realizes stable and high speed operation by adding a transistor for reading to a memory cell.

The diagram illustrates a 1T1R1C1 memory cell structure. It features three horizontal lines at the top: 21: CONTROL LINE, 22: SENSE LINE, and 23: DATA LINE. Two horizontal lines on the right represent word lines: 52: 2ND WORD LINE and 51: 1ST WORD LINE. A substrate structure with a barrier layer (12) is shown. A memory node (30) is connected to the control line. A transistor for writing (1) is connected to the sense line. A transistor for reading (2) is connected to the data line. A memory cell (3) is connected to the word lines. The diagram is labeled with various components and their connections.

Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor memory device formed on a semiconductor substrate and a manufacturing method thereof.

[0002] Semiconductor memories are broadly classified into RAMs (Random-access Memories) and ROMs (Read-only Memories). Of the semiconductor memories, those used in the largest amounts as work storages for computers are dynamic RAMs (hereinafter, referred to as DRAMs).

[0003] In the DRAM, a memory cell for storing information is composed of one storage electric capacitor and a transistor for reading charges stored in the capacitor. Of the RAMs, the DRAM is composed of the minimum number of elements, and therefore, it is suitable for large-scale integration. Accordingly, such semiconductor memories have been produced on a large scale at relatively low costs.

[0004] This DRAM loses information stored therein after an elapse of a certain period of time because charges stored in the electric capacitor are canceled by thermal excitation charges generated in the semiconductor substrate or collision ionization charges due to a strong electric field. The thermal excitation charges and collision ionization charges constitute a leakage current. For this reason, the DRAM is refreshed for restoring the charges before the DRAM loses the information stored therein. In general, the refreshment is performed at intervals of about 100 ms. The reason why the semiconductor memory of this type is called the dynamic RAM is due to such an operational mode.

[0005] In the DRAM, to avoid the above leakage current, internal noise accompanied by operation, and disturbance caused by α -particles, it is substantially difficult to set the level of the storage electric capacitor at a specific value or less. In other words, there exists the minimum signal charge quantity which is, depending on the integration degree of the memory and the configuration of the memory array, estimated to be equivalent to electrons of about a million pieces for a 16 Mbits DRAM and about a hundred thousand pieces for a 16 Gbits DRAM having an integration degree being 1000 times that of the 16 Mbits DRAM.

[0006] In particular, the above leakage current is generated at a pn-junction between the source or drain and the semiconductor substrate. This is because one electrode of the storage electric capacitor is connected to the source or drain of the transistor for reading. Although an actual DRAM product suppresses the collision ionization current due to an electric field by making the pn-junction as fine as possible and making gentle the gradient of an impurity concentration, it is impossible to eliminate the leakage current as is apparent from

the electronic principle of the semiconductor.

[0007] Another problem of the DRAM is that the memory cell has no amplifying effect because information is stored as a quantity of charges and the charges are read out as they are, and accordingly a signal voltage is generally small and the readout rate becomes low.

[0008] The RAM includes a static RAM (SRAM) paired with the DRAM. In general, a memory cell of the SRAM is composed of six transistors, or two resistors and four transistors. These elements constitute flip-flop. The SRAM keeps the storing state insofar as it is applied with a current, and therefore, it does not require refreshment, differently from the DRAM. The SRAM, however, has a size being several times that of the DRAM because the memory cell has a number of composing elements, and accordingly, it is relatively expensive. The SRAM enables high speed operation by an amplifying effect of the memory cell and does not require refreshment, and therefore, it has an advantage in terms of realizing ultra-low power consumption.

[0009] Meanwhile, a usual nonvolatile ROM stores charges by allowing a tunnel current to flow in a storage node surrounded by an insulator. The charge quantity is equivalent to electrons of about a hundred thousand pieces. The insulator generally has a thickness of about 10 nm or more for keeping the memory holding time for 10 years or more. The nonvolatile ROM requires a longer write time as compared with the RAM, and therefore, it cannot be used as the RAM. Further, a current is forcibly applied to the insulator by repeated writing operation, so that the insulator is gradually deteriorated and finally it is converted into a conductor layer, which makes it impossible to hold the memory. Accordingly, in an actual nonvolatile ROM, the number of writing operation is limited to a hundred thousand times.

[0010] In this way, the DRAM, SRAM, and nonvolatile ROM have advantages and disadvantages, and are used in accordance with manners most suitable therefor, respectively.

SUMMARY OF THE INVENTION

[0011] The present invention provides, as described above, a memory having both the features of the usual RAM and nonvolatile memory. The gist of the present invention is to write information in a memory node via a tunnel insulator and to read information from the memory node via a transistor using the memory node as a gate. With this configuration, there can be realized a memory exhibiting an information storing operation similar to that of the usual nonvolatile memory in combination with an amplifying function of a memory cell similar to that of the usual SRAM.

[0012] In other words, an object of the present invention is to provide a semiconductor memory device having a good long-term memory holding characteristic in combination with a stable and high speed RAM operation. Another object of the present invention is to provide

a method of manufacturing such a semiconductor memory device.

[0013] To achieve the above object, a memory cell is composed of, for example, a transistor for writing which is connected to a memory node, and a transistor for reading, which uses the memory node as a gate. This will be described in detail later with reference to preferred embodiments. At this time, a first word line can be connected to the memory node. The transistor for writing can be constituted of a transistor in which a substrate structure having barrier layers, composed of a stack of barrier substrates and barrier layers, is used as the substrate of the transistor and a second word line is used as a gate.

[0014] With this configuration, since the memory node is not connected to the silicon substrate, a leakage current does not allow to flow from the silicon substrate into the memory node, differently from the memory cell of the usual DRAM. Further, since the barrier layers as insulators are present between the memory node and the source connected to a data line of the transistor for writing, it is possible to suppress, differently from the memory cell of the usual DRAM, a sub-threshold current flowing between the source and the drain of the transistor for reading and writing storage charges.

[0015] In addition, these leakage current and the sub-threshold current lose the memory of the DRAM. For this reason, as described above, the DRAM is refreshed. In general, the refreshment is repeated at intervals of about 100 ms.

[0016] In the structure of the present invention, after the power supply is perfectly cutoff, the word line, data line, sense line and control line are all floated, that is, become 0 V. Accordingly, in the structure of the present invention, since any leakage current is not allowed to flow from the substrate, charges in the memory node can be held by making the barrier layer sufficiently thick or making the threshold voltage of the transistor for writing sufficiently high. The structure of the present invention can be thus used as a nonvolatile semiconductor memory device. To make the threshold voltage sufficiently high, the concentration of an impurity doped in the barrier substrate of the transistor for writing may be made high.

[0017] The operational condition to prevent charges of the memory node from being erased during current-carrying to the memory can be achieved by suitably selecting a relationship between a voltage of a non-selection word line and a threshold voltage of a cell writing transistor. This enables an operation similar to that of the usual SRAM.

[0018] Depending on the degree of suppressing the leakage current and the sub-threshold current within the above operational condition, the inventive memory can be realized as a semiconductor device having a characteristic changeable between that of the perfect nonvolatile memory and that of the usual DRAM. In the case of no barrier layer, the inventive memory requires the

refreshment like the DRAM, and in the case where the barrier layer has a thickness comparable to that of a flash memory which is one kind of the nonvolatile memory, there can be realized a nonvolatile memory. Accordingly, the present invention has a large advantage that a desired function can be obtained by selecting the material of the barrier layer and its thickness, and also selecting the material of the barrier substrate and its impurity concentration.

[0019] For example, in the case where the thickness of the barrier layer of the inventive memory is made thin, a sub-threshold current is allowed to flow; however, the magnitude of the sub-threshold current is smaller than that in the usual DRAM because the sub-threshold current can be somewhat suppressed in the inventive memory, and therefore, the inventive memory can act as the usual DRAM in which the time interval of refreshment is made sufficiently longer and thereby a standby power can be reduced. The reduction in standby power enables backup using a battery or the like, and accordingly, the inventive memory can be regarded as a pseudo nonvolatile memory from the viewpoint of the entire configuration including the battery.

[0020] On the other hand, an actual large-scale memory can be realized by arranging a plurality of the memory cells in a matrix, and connecting them to each other by the control line, sense line, data line, first word line, second word line, and the like.

[0021] The basic structure of one example of a memory device of the present invention has a memory cell, and a data line, word line and a sense line connected to the memory cell.

[0022] The memory cell has a memory node for storing charges, a writing element as a path for injecting or discharging charges into or from the memory node, and a reading element for detecting a charge storing state of the memory node. The reading element has a first transistor whose threshold value is changed depending on the charge storing state of the memory node, and the sense line is connected to a source/drain path of the first transistor. The writing element is disposed between the memory node and the data line, and it has a second transistor having a stacked structure of insulators and semiconductor layers and a control electrode formed on the side wall of the stacked structure. Further, the word line is connected to the control electrode.

[0023] Here, the first transistor can be formed on the substrate and the second transistor can be formed on the first transistor. That is to say, when the layout of the substrate plane is viewed from top, the configuration of the first transistor and the configuration of the second transistor are partly or entirely overlapped, and accordingly, the chip area can be reduced.

[0024] At this time, the first transistor is constituted of a field effect transistor, and a gate of the field effect transistor can serve as the memory node. A second control electrode can be provided on the side wall of the gate electrode via an insulator. In this way, the control elec-

trode can be provided on the side wall of the memory node or the transistor. That is to say, the control electrode can extend along in the direction perpendicular to the substrate plane or along a plane crossing the substrate plane.

[0025] According to another example of the present invention, there is provided an apparatus having a MISFET (Metal Insulator Field Effect Transistor), and a stacked structure including insulators and semiconductor regions, which structure is connected to a gate connected to the MISFET. In this example, information is written or erased by injecting or discharging charges into or from the gate via the above stacked structure, and information is read out by means of a sense line connected to a source/drain path of the MISFET. The MISFET is a detecting transistor, and the gate thereof serves as a memory node. The stacked structure connected to the memory node acts as a barrier for controlling injection or discharge of charges into or from the memory node.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026]

Fig. 1 is a sectional view of a first embodiment of the present invention;

Fig. 2 is a circuit diagram of the first embodiment of the present invention;

Fig. 3 is a diagram illustrating the circuit operation of the embodiment of the present invention;

Fig. 4 is a view illustrating an operation of the embodiment of the present invention;

Fig. 5 is a view illustrating an operation of the embodiment of the present invention;

Fig. 6 is a view illustrating an operation of the embodiment of the present invention;

Fig. 7 is a view illustrating an operation of the embodiment of the present invention;

Fig. 8 is a view illustrating an operation of the embodiment of the present invention;

Fig. 9 is a view illustrating an operation of the embodiment of the present invention;

Fig. 10 is a plan view of a second embodiment of the present invention;

Fig. 11 is a sectional view of the second embodiment of the present invention;

Figs. 12 to 16 are views illustrating a sequence of steps of manufacturing the second embodiment of the present invention;

Fig. 17 is a diagram illustrating a memory array of the embodiment of the present invention;

Fig. 18 is a diagram illustrating a circuit operation of the memory array of the embodiment of the present invention;

Fig. 19 is a plan view of the first embodiment of the present invention;

Figs. 20 to 23 are views of a sequence of steps of

manufacturing the first embodiment of the present invention;

Fig. 24 is a sectional view of the first embodiment of the present invention;

Fig. 25 is a sectional view of a third embodiment of the present invention;

Figs. 26 to 28 are views of a sequence of steps of manufacturing the third embodiment of the present invention;

Fig. 29 is a circuit diagram of a fourth embodiment of the present invention;

Fig. 30 is a sectional view of the fourth embodiment of the present invention;

Fig. 31 is a diagram showing a memory cell circuit of a fifth embodiment of the present invention;

Fig. 32 is a diagram showing a memory cell circuit of the fifth embodiment of the present invention;

Fig. 33 is a diagram illustrating a circuit operation of the memory cell of the fifth embodiment of the present invention;

Fig. 34 is a plan view of a memory cell of the fifth embodiment of the present invention; and

Fig. 35 is a sectional view of the memory cell of the fifth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] Figs. 1 and 2 show the structure and the circuit of a first embodiment, respectively.

[0028] Fig. 1 shows the basic structure of the present invention. Reference numeral 10 denotes a p-type silicon substrate having a resistivity of about 10 Ω -cm; 60 is a field insulator; 21 is a control line formed of an n⁺-region; and 22 is a sense line formed of an n⁺-region. A first gate insulator 41 is formed on the surface of the silicon substrate 10, and a memory node 30 is formed on the first gate insulator 41. A second gate insulator 42 is formed around the side wall of the memory node 30, and a first word line 51 is formed so as to cover the second gate insulator 42. An electric capacitor is thus formed, via the second insulator 42, between the first word line 51 and the memory node 30. On the memory node 30 is formed a substrate structure 12 having barrier layers, which is of a multi-layer structure composed of barrier substrates 11 made from polycrystalline silicon or amorphous silicon and barrier layers 70 made from silicon oxide, silicon nitride or the mixture thereof, that is, silicon oxide/nitride. A third gate insulator 43 is formed around the side surface of the substrate structure 11 having barrier layers. A second word line 52, which serves as a gate of a transistor using the substrate structure 7 as a substrate, is formed on the side surface of the third gate insulator 43. An n⁺-type source region 24 is formed on the uppermost portion of the substrate structure 12 having barrier layers, and a data line 23 is formed in such a manner as to be connected to the n⁺-type source region 24.

[0029] Fig. 2 shows the circuit and the connection of

the above memory cell composed of these layers and the substrates. By arranging the memory cells in a matrix of m -columns \times n -rows into a memory array, there can be obtained a large scale memory. For example, a 1-Mbit memory can be obtained by arranging the memory cells in a matrix of 1024 columns \times 1024 rows.

[0030] As shown in Figs. 1 and 2, the memory cell is composed of a transistor 1 for writing which is connected to the memory node 30 and a transistor 2 for reading which takes the memory node 30 as its gate. Also as shown in Fig. 1, the transistor 1 for writing is a transistor which takes, as a substrate, the substrate structure 12 composed of a stack of the barrier substrates 11 and the barrier layers 70 and which takes the second word line 52 as its gate.

[0031] With this configuration, since the memory node is not connected to the silicon substrate, any leakage current does not flow from the silicon substrate into the memory node, differently from the memory cell of the usual DRAM; and further, since the barrier layers as the insulators are provided between the memory node and the source, connected to the data line, of the transistor for writing, it is possible to suppress a sub-threshold current which flows, as described above, between a source and a drain of a transistor for reading and writing of stored charges in the memory cell of the usual DRAM.

[0032] According to the structure of the present invention, after the power supply is perfectly cutoff, the word line, data line, sense line, and control line are all floated, that is, become 0 V, and in this case, any leakage current does not flow from the silicon substrate into the memory node and also the electric charges in the memory node can be kept by making the barrier layers sufficiently thick or making the threshold voltage of the transistor for writing sufficiently high. Accordingly, a nonvolatile memory can be realized using such a structure of the present invention. In addition, the threshold voltage of the transistor for writing can be made sufficiently high by increasing the concentration of an impurity doped in the barrier substrate 11.

[0033] An operational condition, which does not allow the charges in the memory node to be lost during current-carrying in the memory, can be attained by suitably setting a relationship between a voltage of a non-selection word line and the threshold voltage of the transistor for writing. This allows the memory to be acted just as the usual SRAM.

[0034] Within the above operational condition, the characteristic of the inventive memory is variable between that of the perfect nonvolatile memory and that of the usual DRAM by changing the degree of suppressing the leakage current and the sub-threshold current. If the inventive memory has no barrier layer 70, it must be refreshed like the usual DRAM cell. On the other hand, if the inventive memory has the barrier layer 70 having a large thickness comparable to that of a flash memory which is one kind of nonvolatile memory, it can act as a

nonvolatile memory. Accordingly, the present invention has a large advantage in that a desired function can be obtained by selecting the material of the barrier layer 70 and its thickness and also the material of the barrier substrate 11 and its impurity concentration.

[0035] To be more specific, in the case where the thickness of the barrier layer 70 of the inventive memory is made thin, a sub-threshold current is allowed to flow; however, the magnitude of the sub-threshold current is smaller than that in the usual DRAM because the sub-threshold current can be somewhat suppressed in the inventive memory, and therefore, the inventive memory can act as the usual DRAM in which the time interval of refreshment is made sufficiently longer and thereby a standby power can be reduced. The reduction in standby power enables backup using a battery or the like, and accordingly, the inventive memory can be regarded as a pseudo nonvolatile memory from the viewpoint of the entire configuration including the battery.

[0036] On the other hand, an actual large-scale memory can be realized by arranging a plurality of the memory cells in a matrix, and connecting them to each other by the control line 21, sense line 22, data line 23, first word line 51, second word line 52, and the like.

[0037] Fig. 3 is a timing chart showing writing and reading operations to and from the memory cell of the present invention. In this timing chart, it is assumed that the threshold voltages of the transistor for writing and the transistor for reading are taken as 2 V and 1.2 V, respectively; and a voltage coupled to the memory node 30 by the electric capacitor formed, via the first gate insulator 41, between the first word line 51 and the memory node 30 is taken as 0.8 V.

[0038] The writing operation is performed by applying pulses to the second word line, and applying a writing information voltage 1 V (corresponding to information "1") or 0 V (corresponding to information "0") applied to the data line to the memory node. Here, since the voltage of the word line is as sufficiently high as 3 V or more, the voltage of the data line is written to the memory node as it is without being affected by the threshold voltage (2 V) of the transistor for writing.

[0039] The reading operation is performed by applying pulses to the first word line and the control line, and discriminating whether or not the transistor for reading is made conductive. To be more specific, it is discriminated whether the information is "1" or "0" on the basis of the presence or absence of a current flowing in the sense line or the presence or absence of a micro-voltage appearing in the sense line. For example, the voltage of the memory node is increased to 1.8 V or 0.8 V by applying pulses to the first word line, and in this case, since the voltage of the control line is 0 V and the threshold voltage of the transistor for reading is 1.2 V, if the information "1" is stored in the memory node, the transistor for reading is made conductive, and if the information "0" is stored in the memory node, the tran-

sistor for reading is made non-conductive. By connecting an impedance (MOS transistor or resistor) of 2 V to the other end of the sense line, upon readout of the information "1", the voltage of the sense line is reduced a micro-voltage δ (about 200 mV) from 2 V; while upon readout of the information "0", the voltage of the sense line is left as 2 V. Such a difference in voltage is discriminated by a detection circuit connected to the sense line.

[0040] It is to be noted that the reading operation is not obstructed by a number of non-selection cells connected to the same sense line and control line and arranged in the direction of the sense line. The reason for this is that since the first word lines of the non-selection cells are not applied with pulses, the memory node of each of the non-selection cells is 1 V or 0 V which is lower than the threshold voltage of the transistor for reading, and accordingly the transistor for reading in each of the non-selection cells is in the non-conductive state.

[0041] In the memory cell structure of the present invention, as described above, the leakage current at the pn-junction in the cell little occurs and also a resistance against soft errors due to the incidence of α -particles is high. However, depending on the magnitude of the threshold voltage of the transistor for writing, information charges possibly flow into the data line via the transistor for writing, thereby causing breakage of the information. If the threshold voltage is as sufficiently high as about 2 V, even if the power supply is cutoff and the word line and the like are floated and become 0 V, the nonvolatile operation is possible because the transistor for writing is made nearly perfectly non-conductive; and further, charges in the non-selection cells do not flow in the data line even upon random operation during current-carrying. As a result, in the case where the threshold voltage is sufficiently high, there can be provided a memory not requiring refreshment like the usual SRAM.

[0042] However, depending on the configuration of the barrier layer, or in the case where it is desired to lower the voltage applied to the second word line for low voltage operation, there inevitably occur circumstances in which the threshold voltage is lowered. However, if the threshold voltage is excessively lowered, charges in the memory node start to flow in the data line via the transistor for writing. In such a case, like the usual DRAM, the memory must be refreshed to keep the stored information. The refreshing operation is performed by reading the information in the memory cell by a detection circuit connected to the sense line, converting the result into a writing voltage on the data line, and re-writing it to the memory cell. Of course, the memory cell of the present invention has an advantage that since the leakage current at the pn-junction in the memory cell little occurs, the information holding time can be correspondingly prolonged as compared with the usual DRAM cell.

[0043] The operations of transistors, each using a substrate having one or more barrier layers, will be

described with reference to Figs. 4 to 9.

[0044] Fig. 4 shows the structure of a transistor using a substrate having a barrier layer, in which a single barrier layer having a thickness of t_b is inserted in a substrate of the usual n-channel transistor at an intermediate portion between a source and a drain.

[0045] Fig. 5 shows the energy band structure of the transistor shown in Fig. 4. In general, the barrier layer is an insulator having a forbidden band energy gap E_g . For this n-channel transistor using the substrate having the single barrier layer, there exists a conduction band of the barrier layer at a level which is higher an electron affinity "c" than that of the conductor E_c .

[0046] In the state shown in Fig. 5 in which no gate voltage is applied, in order to allow a current between the source and the drain of the transistor, it is required to satisfy either a condition that the barrier layer is thin enough to allow a tunnel current to directly pass through the barrier layer or a condition that electrons have energies large enough to flow over the electron affinity "c". The transistor actually exhibits a current form intermediate between the above conditions depending on the thickness of the barrier layer.

[0047] Fig. 6 shows the energy band structure in the case where a positive gate voltage is applied to the structure shown in Fig. 5. The current flowing between the source and the drain of the transistor can be controlled by a gate G, as shown in Fig. 6. Like the general transistor, when a positive voltage larger than the threshold voltage of the transistor is applied, the energy band is largely reduced toward the gate plane, to thereby increase the current flowing between the source and the drain. Further, the energy of the conduction band of the barrier insulator is made lower than the energy level of the source although the electron affinity "c" is kept constant, so that the current is easy to flow over the barrier layer. The present invention applies such a principle and uses the drain of the transistor as the memory node of the memory cell.

[0048] Fig. 7 shows the energy band structure of a transistor using a substrate having two layers of barrier insulators. In general, in the case of provision of multi-layered insulators, the probability allowing electrons to tunnel through the multi-layered insulators is equal to that allowing electrons to tunnel through a single insulator having a thickness equal to the total thickness of the multi-layered insulators. Accordingly, in the case where it is difficult to form a single thick barrier insulator, there may be provided multi-layered barrier insulators having a desired total thickness.

[0049] Fig. 8 shows another structure of the present invention, in which a substrate having a barrier layer is sandwiched by two gates. Since no voltage is applied from the exterior to the substrate having the barrier layer as in the structure shown in Fig. 1, the substrate having the barrier layer is in the so-called floating state.

[0050] Fig. 9 shows the energy band structure of the transistor using the substrate having the barrier layer

shown in Fig. 8. Since the substrate having the barrier layer is in the floating state, if the concentration of an impurity doped in the substrate is kept constant in the direction parallel to the source and the drain, as shown in Fig. 9, any electric field is not present in the direction parallel to the source and the drain, and thereby the energy band is made flat in the direction parallel to the source and the drain. In this case, the current flowing between the source and the drain is equalized over the substrate, and consequently, as compared with the case shown in Fig. 6 where the current flows on the surface of the substrate directly under the gate, the reduction in mobility of carriers, that is, electrons becomes small for the n-channel transistor. As a result, there can be realized a transistor having a high mutual conductance.

[0051] As will be fully described with reference to the later embodiment of the present invention, since the structure shown in Figs. 8 and 9 does not require an electrode for applying an external voltage to the substrate having the barrier layer, there can be obtained advantages that not only the structure of the memory cell can be simplified but also the plane area can be reduced.

[0052] The substrate structure using the two barrier layers shown in Fig. 7 can be applied to the transistor shown in Figs. 8 and 9. In this case, the same effect can be obtained.

[0053] Although the n-channel transistor formed on the p-type substrate is used for the configurations shown in Figs. 3 to 9 for simplification of description of the operation of the present invention, the present invention is not limited to the conducting type of the substrate insofar as the current flowing between the source and the drain can be essentially controlled by the gate. That is to say, in the present invention, there can be used various types of substrates, for example, a very lightly doped n⁺-type substrate, an intrinsic type substrate having an extremely high resistivity, and a p-type substrate. If it is desired to control the substrate by applying a low voltage thereto, the impurity concentration near that of the intrinsic type may be selected.

[0054] On the other hand, for the p-type barrier substrate, a pn-junction is formed between the drain and the barrier substrate, and in this case, if a depletion layer is present, thermal excitation charges are generated at the depletion layer, causing breakage of the stored information. Accordingly, in this case, the kind of an impurity and the concentration thereof may be controlled to minimize the thermal excitation charges.

[0055] Fig. 10 is a plan view of a memory cell according to a second embodiment of the present invention. This embodiment is characterized in that a memory node 30 is flatly extended and a first word line 51 is not located directly under a second word line 52. With this configuration, the overall height of this embodiment is made lower than that of the first embodiment, and therefore, it is easier to form this embodiment as compared

with the first embodiment. Fig. 11 is a sectional view taken on line A-A' of the memory cell shown in Fig. 10; and Fig. 12 is a sectional view taken on line B-B' of the memory cell shown in Fig. 10. In addition, parts corresponding to those shown in Fig. 1 are denoted by the same reference numerals as those shown in Fig. 1.

[0056] Figs. 13 to 16 show sequential steps of forming the second embodiment of the present invention.

[0057] As shown in Fig. 13, n⁺-type regions 21 and 22 are formed in a p-type silicon substrate having a resistivity of about 10 Ω -cm by the usual photo-etching process and ion implantation process. A field insulator 60 made from a silicon oxide layer having a thickness of 500 nm is then selectively formed by a LOCOS (Local Oxidation of Silicon) process using a silicon nitride layer selectively formed for prevention of oxidation.

[0058] As shown in Fig. 14, a silicon oxide layer having a thickness of 10 nm is formed on the surface of the substrate 10 at 1000°C. This silicon oxide layer is taken as a first gate insulator 41. On the first gate insulator 41 is selectively formed a layer of polycrystalline silicon doped with an n⁺-type impurity, which layer is taken as a memory node 30. Then, as already shown in Fig. 11, a first interlayer insulator 61 having a thickness of 500 nm is formed by CVD; a portion of the first interlayer insulator 61, positioned on a certain area of the memory node 30, is removed; and a silicon oxide layer having a thickness of 10 nm is formed on the surface of the memory node 30 at the above area from which the first interlayer insulator 61 is removed. This silicon oxide layer is taken as a second gate insulator 42. On the second gate insulator 42 is selectively formed a layer of conductive polycrystalline silicon, which layer is taken as a second word line 52.

[0059] As shown in Fig. 15, a barrier substrate 11 made from polycrystalline silicon or amorphous silicon is formed on the memory node 30 to a thickness of 500 nm, followed by heat-treatment at 1000°C in an oxygen atmosphere containing ammonia or nitrogen to form a silicon oxide/nitride layer having a thickness of 5 nm, which layer is taken as a barrier layer 70. In Fig. 12, three barrier substrates 11 and two barrier layers are formed. The minimum number of the barrier substrates is two, and the minimum number of the barrier layer 70 is one.

[0060] Then, as already shown in Fig. 12, a second gate insulator 42 having a thickness of 10 nm is formed by the usual thermal oxidation process at 1000°C, and a first word line 51, represented by a layer of polycrystalline silicon doped with an impurity, W or Mo or a silicide layer thereof, is formed on the second gate insulator 42.

[0061] As shown in Fig. 16, a silicon oxide/nitride layer having a thickness of 5 nm is formed by heat-treatment at 1000°C in an oxygen atmosphere containing ammonia or nitrogen, which layer is taken as a third gate insulator 43. Then, a layer of conductive polycrystalline silicon is formed over the entire surface, and is subjected to anisotropic dry etching in a state in which a

photoresist is left on a portion at which a second word line 52 is to be formed, to form a second word line 52 at the desired portion. At this time, the second word line 52 remains on the side wall of the projecting multi-layered substrate structure 7 having the barrier substrates 11 and the barrier layers 70 even if the side wall of the substrate structure 7 is not covered with the photoresist. The reason for this is that the etching does not proceed in the horizontal direction because of the use of the strong anisotropic dry etching. This means that the second word line 52 can be formed in self-alignment around the substrate structure 7 having the barrier layers.

[0062] As already shown in Figs. 11 and 12, a drain region 24 doped with arsenic or phosphorous is formed, and then like the first interlayer insulator 61, a second interlayer insulator 62 is formed. Then, an opening is formed in the second interlayer insulator 62, and a data line 23 made from aluminum or the like is selectively formed in the opening. In this way, the memory cell of the present invention, whose circuit is shown in Fig. 2, can be realized. In comparing this memory cell with the first embodiment, since in this memory cell the first word line 51 is formed on the plane adjacent to the second word line 52, the plane area becomes larger. To be more specific, in this memory cell, assuming that the processing dimension of all patterns is taken as F and the pattern alignment accuracy is taken as $2/F$, the theoretical area becomes $13.5 (=3.0 \times 4.5) F^2$.

[0063] Fig. 17 shows another embodiment of the present invention in which memory cells are arranged in a matrix to constitute a memory array. In this embodiment, the sense line and the control line adjacent to each other are shared to reduce the entire area.

[0064] Fig. 18 is a timing chart showing a circuit operation of the memory cell shown in Fig. 17. As shown in Fig. 18, the writing operation is performed by applying pulses to a second word line (WW_1) and applying desired wiring information voltages to respective data lines (D_1, D_2, \dots) of a plurality of cells ($MC_{11}, MC_{12}, MC_{13}, \dots$) connected to the second word line. That is to say, the plurality of cells are simultaneously, collectively written. The reading operation is performed, in consideration of the fact that sense lines ($S_1, S_2, S_3, S_4, \dots$) are shared by the adjacent cells in the word line direction, by selectively driving alternate control lines (C_1, C_2, \dots) with address signals in order to eliminate interference between the cells. For example, Fig. 18 shows an example in which the odd-numbered control lines are driven. The pieces of information readout from the cells $M_{11}, M_{12}, M_{15}, M_{16}$ are led into the sense lines S_1, S_2, S_3 and S_4 , and no information is readout from the MC_{13} and M_{14} . Although the memory node of each of the cells MC_{13} and MC_{14} is 1.8 V or 0.8 V, the transistor for reading in each cell is made non-conductive because the voltage of the control line C_2 is 2 V, the voltage of each of the sense lines S_2 and S_3 is 2V-5 (about 200 mV), and the threshold voltage of the transistor for reading is

1.2 V.

[0065] In addition, the sense lines may be respectively provided to the adjacent cells. In this case, although the area of the memory cell becomes larger, there has an advantage in simplifying the circuit design because there is no need to decode the control lines with address signals for selective drive of the control lines.

[0066] Fig. 19 is a plan view of the first embodiment of the present invention, similar to the plan view of the second embodiment shown in Fig. 10. In this embodiment, the theoretical area of the memory cell becomes $9.0 (=3.0 \times 3.0) F^2$, which is largely reduced as compared with that of the second embodiment shown in Fig. 10.

[0067] Figs. 20 to 23 show sequential steps of forming the first embodiment of the present invention. As shown in Fig. 20, n^+ -type regions 21 and 22 are formed in a p -type silicon substrate having a resistivity of about $10 \Omega\text{-cm}$ by the usual photo-etching process and ion implantation. A field insulator 60 made from a silicon oxide layer having a thickness of 500 nm is selectively formed by LOCOS (Local Oxidation of Silicon) using a silicon nitride layer selectively formed for prevention of oxidation.

[0068] As shown in Fig. 21, a silicon oxide layer having a thickness of 10 nm is formed at 1000°C on the surface of the substrate 10, which layer is taken as a first gate insulator 41. On the first gate insulator 41 is selectively formed a layer of polycrystalline silicon doped with an n^+ -type impurity, which layer is taken as a memory node 30. Then, extension portions of the n^+ -type regions 21 and 22 are formed in self-alignment with the memory node 30 by ion implantation, to thereby realize the so-called LDD (Lightly Doped Drain) structure.

[0069] As shown in Fig. 22, a silicon oxide layer having a thickness of 10 nm is formed at 1000°C on the surface of the memory node 30, which layer is taken as a second gate insulator 42. A layer of conductive polycrystalline silicon is then formed over the entire surface, and is subjected to anisotropic dry etching in a state in which a photoresist is left on a portion at which a first word line 51 is to be formed, to form a first word line 51 at the desired portion. At this time, the first word line 51 remains on the side wall of the projecting memory node 30 even if the side wall of the memory node 30 is not covered with the photoresist. This is because the etching does not proceed in the horizontal direction resulting from the use of the strong anisotropic dry etching. This means that the first word line 51 can be formed in self-alignment around the memory node 30. Then, a first interlayer insulator 61 having a thickness of 500 nm is formed by CVD, followed by planarization of the entire surface of the first interlayer insulator 61 using a CMP (Chemical Mechanical Polishing) process, to expose the uppermost surface of the memory node 30.

[0070] As shown in Fig. 23, a barrier substrate 11 made from polycrystalline silicon or amorphous silicon is formed to a thickness of 500 nm, followed by heat-treatment at 1000°C in an oxygen atmosphere contain-

ing ammonia or nitrogen to form a silicon oxide/nitride layer having a thickness of 5 nm, which layer is taken as a barrier layer 70. Then, a silicon oxide/nitride layer having a thickness of 5 nm is formed by heat-treatment at 1000°C in an oxygen atmosphere containing ammonia or nitrogen, which layer is taken as a third gate insulator layer 43. Then, a layer of conductive polycrystalline silicon is formed over the entire surface, and is subjected to anisotropic dry etching in a state in which a photoresist is left on a portion at which a second word line 52 is to be formed, to form a second word line 52 at the desired portion. At this time, the second word line 52 remains on the side wall of the projecting multi-layered substrate structure 7 having the barrier substrates 11 and the barrier layers 70 even if the side wall of the substrate structure 7 is not covered with the photoresist. The reason for this is that the etching does not proceed in the horizontal direction because of the use of the strong anisotropic dry etching. This means that the second word line 52 can be formed in self-alignment around the substrate structure 7 having the barrier layers.

[0071] As already shown in Fig. 1, a drain region 24 doped with arsenic or phosphorous is formed, and then like the first interlayer insulator 61, a second interlayer insulator 62 is formed. Then, an opening is formed in the second interlayer insulator 62, and a data line 23 made from aluminum or the like is selectively formed in the opening. In this way, the memory cell of the present invention, whose circuit is shown in Fig. 2, can be realized. Fig. 1 is a sectional view taken on line A-A' of Fig. 19; and Fig. 24 is a sectional view taken on line B-B' of Fig. 19. In this embodiment, as described above, the theoretical area of the memory cell is $9F^2$. In other words, according to this embodiment, the smallest cell can be realized.

[0072] Fig. 25 shows a third embodiment of the present invention, in which a memory node 30 and a substrate structure 7 having barrier substrates 11 and barrier layers 70 are collectively formed. In this embodiment, a finer structure can be realized by eliminating mask alignment required for the memory node 30 and the substrate structure 7 at the photo-etching step in the first embodiment.

[0073] Figs. 26 to 28 illustrate part of sequential steps of forming the third embodiment. As shown in Fig. 26, after the memory node 30 and the substrate structure 7 having barrier layers are collectively formed, a silicon oxide/nitride layer having a thickness of 5 nm is formed by heat-treatment at 1000°C in an oxygen atmosphere containing ammonia and nitrogen, which layer is taken as a second gate insulator 42. Then, a layer of conductive polycrystalline silicon is formed over the entire surface by CVD or the like. Further, an etching protective layer made from photoresist or polyimide is formed by CVD, followed by etch-back over the entire surface to thin the layer to a specific thickness, to obtain an etching protective layer 63.

[0074] The conductive poly-silicon layer is etched using the etching protective layer 63 as a mask, to form a first word line 51 as shown in Fig. 23. After that, the steps having described with reference to Figs. 23, 24 and 1 are repeated, to realize the structure shown in Fig. 21.

[0075] Fig. 29 shows a circuit of a fourth embodiment of the present invention. In this embodiment, differently from the circuit having described with reference to Fig. 2 in which the first word line 51 and the second word line 52 are separately controlled, the first word line 51 and the second word line 52 are integrated into only the first word line 51. Such integration of the first and second word lines 51 and 52 becomes possible by suitably selecting the threshold voltages of the transistor 1 for writing and the transistor 2 for reading and the voltage applied to the first word line 51.

[0076] Fig. 30 shows a memory cell structure of the fourth embodiment. The memory cell structure in the fourth embodiment can be made simpler and finer in structure and also simpler in manufacture than each of the first, second and third embodiments.

[0077] Fig. 31 shows the circuit of a fifth embodiment of the present invention.

[0078] Fig. 32 is a memory array circuit of the fifth embodiment.

[0079] Fig. 34 is a timing chart showing the operation of the fifth embodiment. The structure of this embodiment is easy to be manufactured because a step-up capacitor and a word line for driving it are omitted. In this embodiment, the control line used in the previous embodiments is rearranged in parallel to the word line, which control line is taken as a first word line. Here, the operation will be described in a condition that only the threshold voltage of the transistor for reading is changed into 0.5 V. The information is written as "1 V" or "0 V" in a memory node by the writing operation. The reading operation for each of the memory cells MC_{11} and MC_{12} is performed by setting the voltage of the first word line (RW_1) at 0 V. If the voltage of the memory node is 1 V, the transistor for reading is made conductive, while if it is 0 V, the transistor for reading is made non-conductive, and accordingly, like the previous embodiments, it can be discriminated whether the information is "1" or "0". It is to be noted that the transistors for reading in the memory cells MC_{21} and MC_{22} , which are made non-conductor, do not exert adverse effect on the reading operation of the memory cells MC_{11} and MC_{12} .

[0080] Fig. 34 is a plan view of the memory cell of the fifth embodiment of the present invention, and Fig. 35 is a sectional view taken on line A-A' of Fig. 34.

[0081] As described above, the description of the previous embodiments of the present invention is limited to the memory cell and a memory array composed of the memory cells. However, the actual memory further includes direct peripheral circuits directly connected to the array, such as a sense amplifier and a decoder; and

indirect peripheral circuits for achieving functions as the memory, such as a logic circuit and an input/output circuit. To suppress a sub-threshold current, the gate length of a memory array is generally set longer than that of a direct peripheral circuit.

[0082] In the embodiments of the present invention, with respect to a direct peripheral circuit and an indirect peripheral circuit, if the source/drain of the transistor, for example, shown in Fig. 14, are directly used for the diffusion layer wirings, mask alignment is required because the memory node 30 as the gate is formed later, so that the transistor performance is generally degraded. Accordingly, as shown in Fig. 21, it is advantageous to use the source/drain (expressed by the control line 21 and the sense line 22 in Fig. 21) formed in self-alignment in the memory node 30.

[0083] However, in general, these lines are formed separately from the memory array for the reason of increasing the degree of freedom, thereby easily attaining a desired performance. The method of forming these lines is performed by adopting a general self-alignment silicon gate structure or LDD (Lightly Doped Drain) structure in which the concentration of an impurity near the source/drain is lowered. The present invention does not specify such a method of forming the transistor.

[0084] As described above, the present invention provides a memory having a characteristic of the usual RAM in combination with a characteristic of the usual nonvolatile memory. That is to say, there can be realized a memory exhibiting an information storing operation similar to that of the usual nonvolatile memory in combination with an amplifying function of a memory cell similar to that of the usual SRAM. In other words, the effect of the present invention is to provide a so-called "non-volatile RAM" having a good long-term memory holding characteristic in combination with a stable and high speed RAM operation.

Claims

1. A semiconductor memory device comprising:

a memory node constituted of a gate of a transistor formed on a semiconductor substrate; and
a multi-layer structure having semiconductor regions and barrier insulators, said structure being connected to said memory node; wherein writing and/or erasing of charges are performed via said barrier insulators.

2. A semiconductor memory device according to claim 1, wherein said memory node and said multi-layer structure having semiconductor regions and barrier insulators are superimposed to each other in the direction perpendicular to said semiconductor substrate.

3. A semiconductor memory device according to claim 1, wherein an electrode is provided on said memory node via an insulator for reading a signal of a memory cell.

4. A semiconductor memory device according to claim 1, wherein said devices are arranged in a matrix.

5. A semiconductor memory device comprising:

a memory cell, and a data line, a word line and a sense line connected to said memory cell; wherein said memory cell has a memory node for storing charges, a writing element as a path through which charges are injected or discharged into or from said memory node, and a reading element for detecting a charge storing state of said memory node;

said reading element has a first transistor whose threshold value is changed depending on the charge storing state of said memory node;

said sense line is connected to a source/drain path of said first transistor, and said writing element is disposed between said memory node and said data line;

said writing element has a second transistor having an insulator, a stacked structure of semiconductor layers, and a control electrode formed on a side wall of said stacked structure; and

said word line is connected to said control electrode.

6. A semiconductor memory device according to claim 5, wherein said first transistor is formed on a substrate, and said second transistor is arranged on said first transistor.

7. A semiconductor memory device according to claim 6, wherein said first transistor is constituted of a field effect transistor, and a gate electrode of said field effect transistor serves as said memory node.

8. A semiconductor memory device according to claim 7, wherein a second control electrode is provided on a side wall of said gate electrode via an insulator.

9. A semiconductor memory device comprising:

a MISFET formed on a semiconductor substrate; and

a stacked structure having semiconductor regions and insulators, said stacked structure being connected to a gate of said MISFET transistor;

wherein information is written or erased by

injecting or discharging charges into or from said gate via said stacked structure, and information is read by a sense line connected to a source/drain path of said MISFET transistor.

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FIG. 1

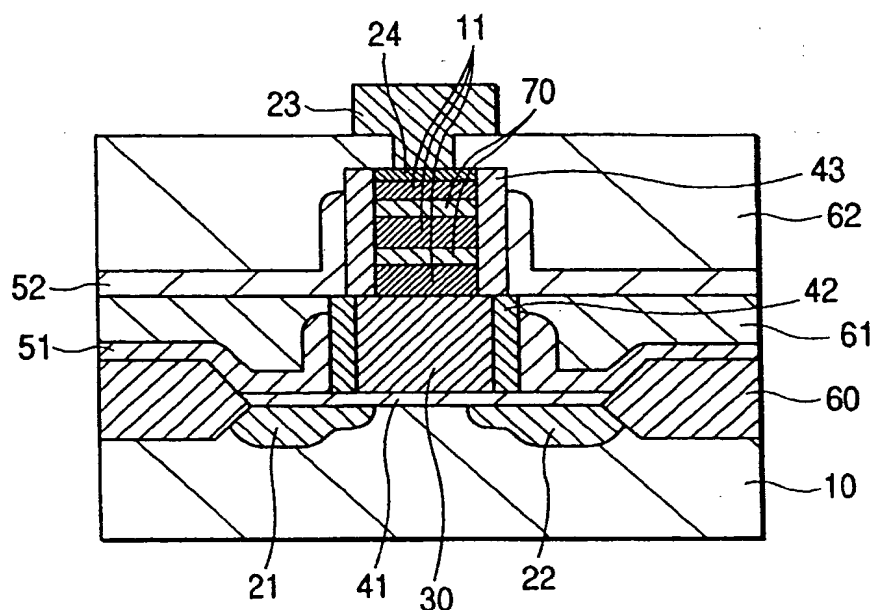


FIG. 2

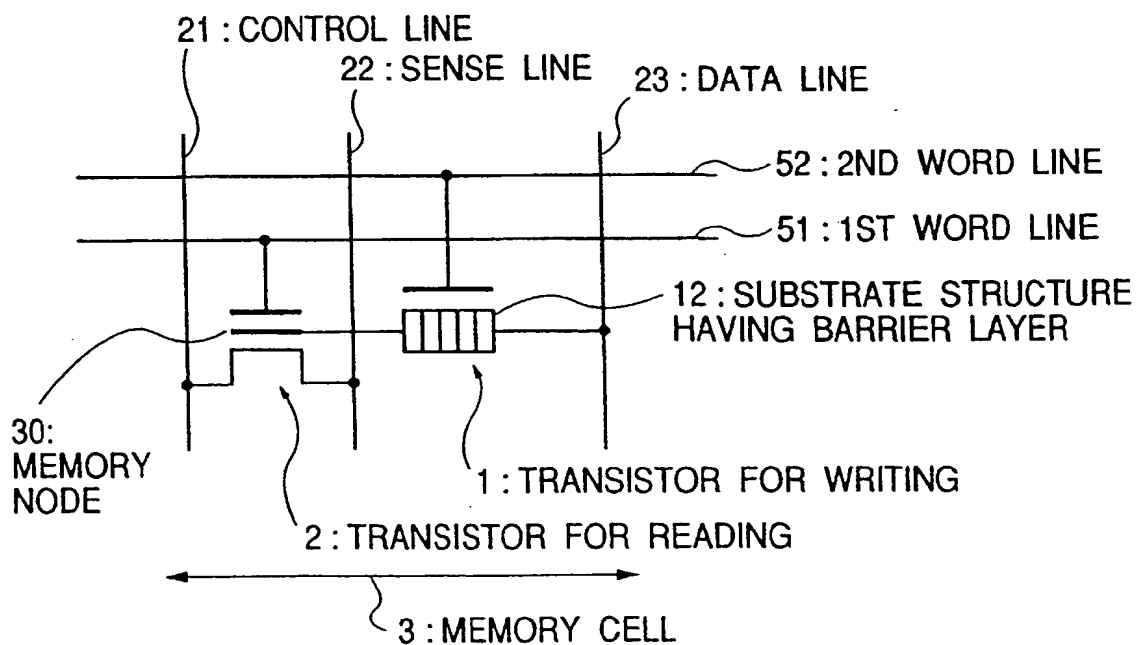


FIG. 3

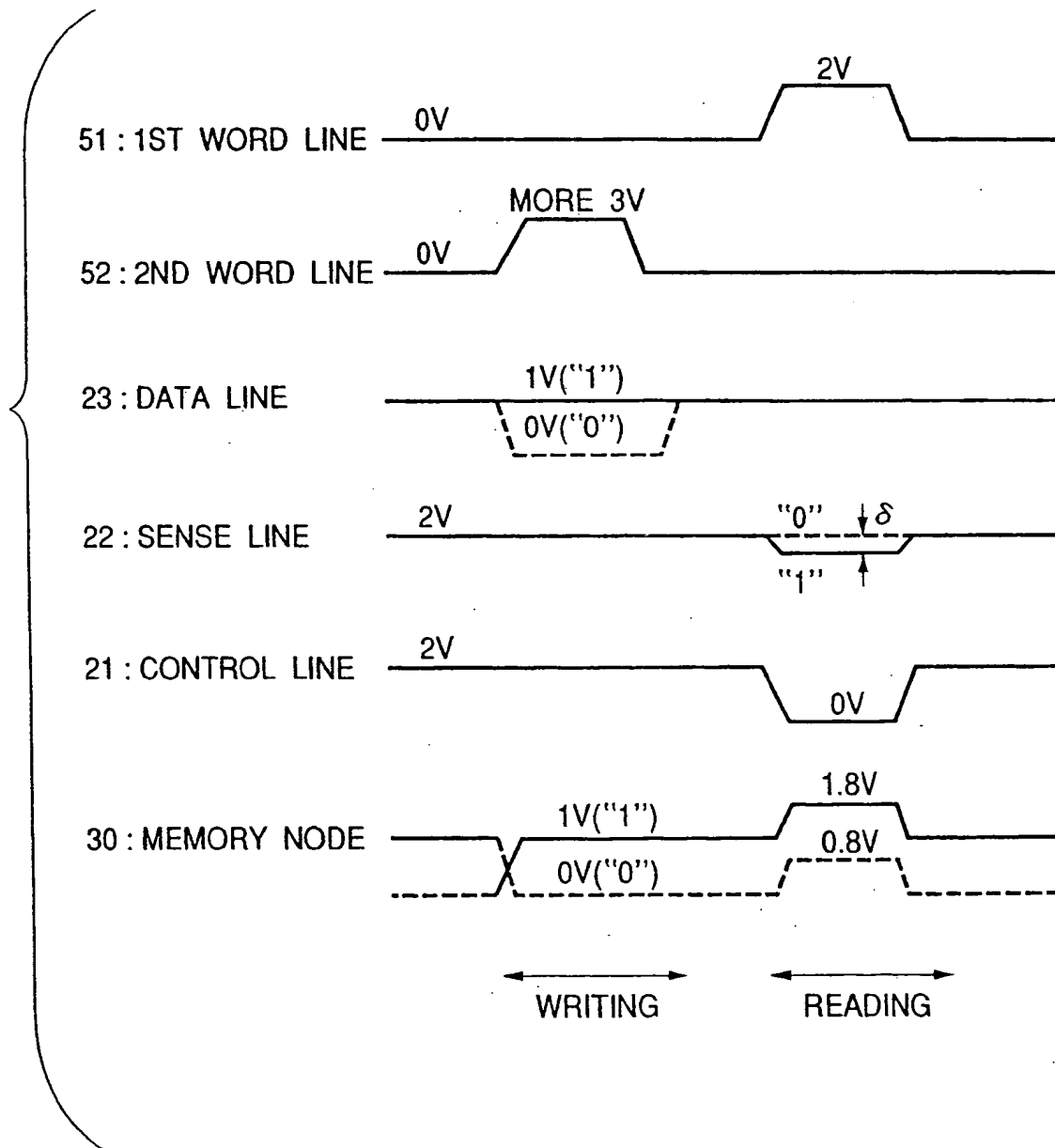


FIG. 4

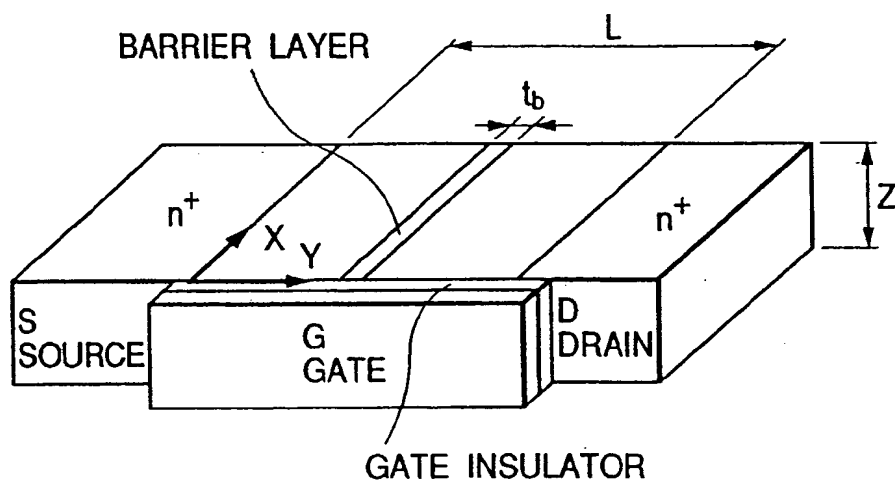


FIG. 5

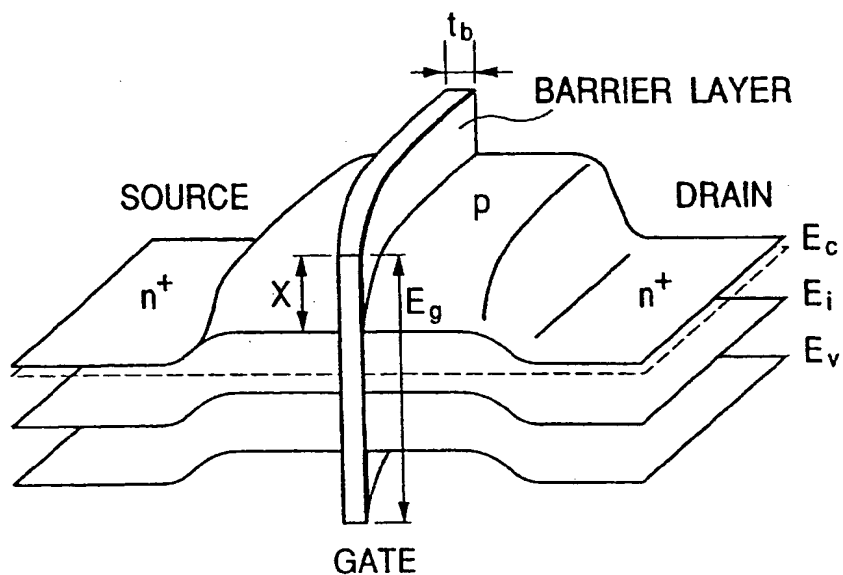


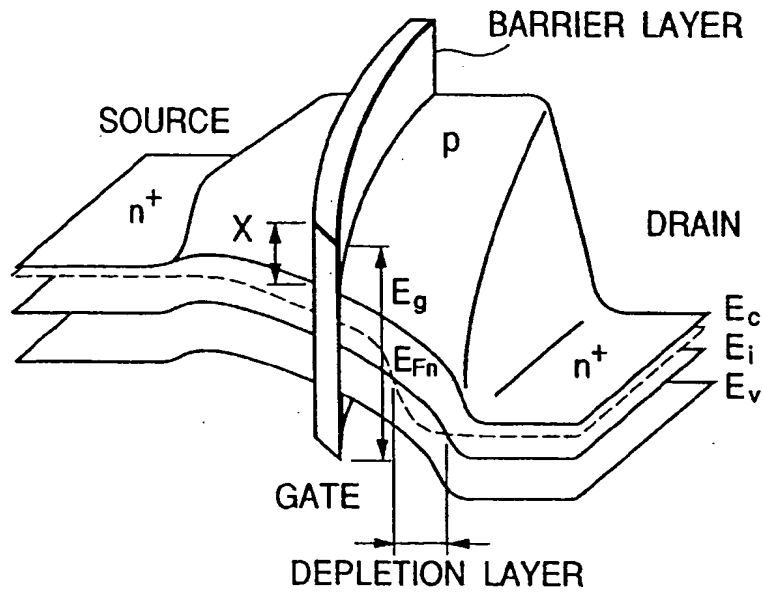
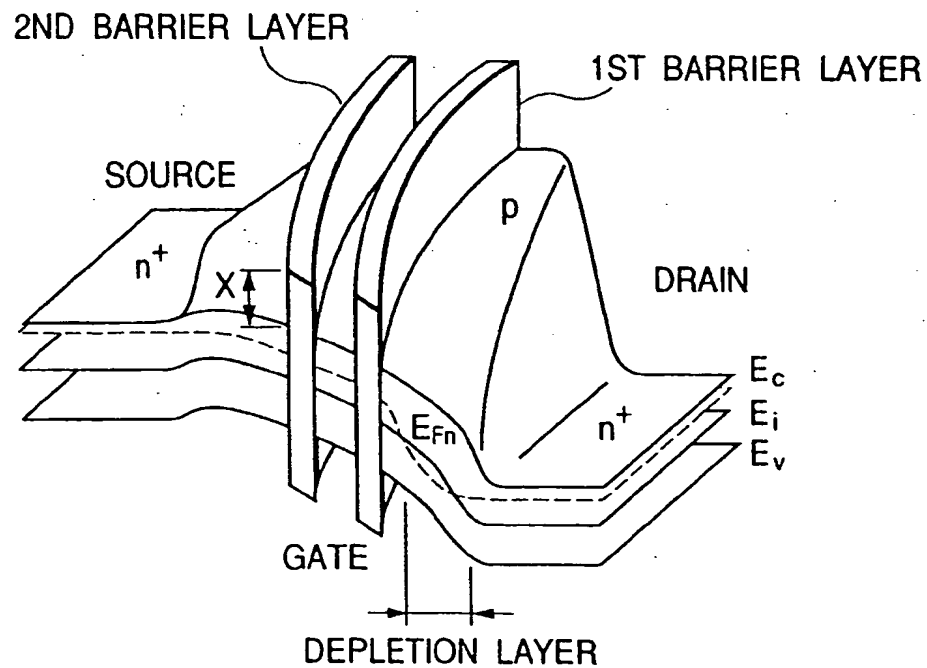
FIG. 6**FIG. 7**

FIG. 8

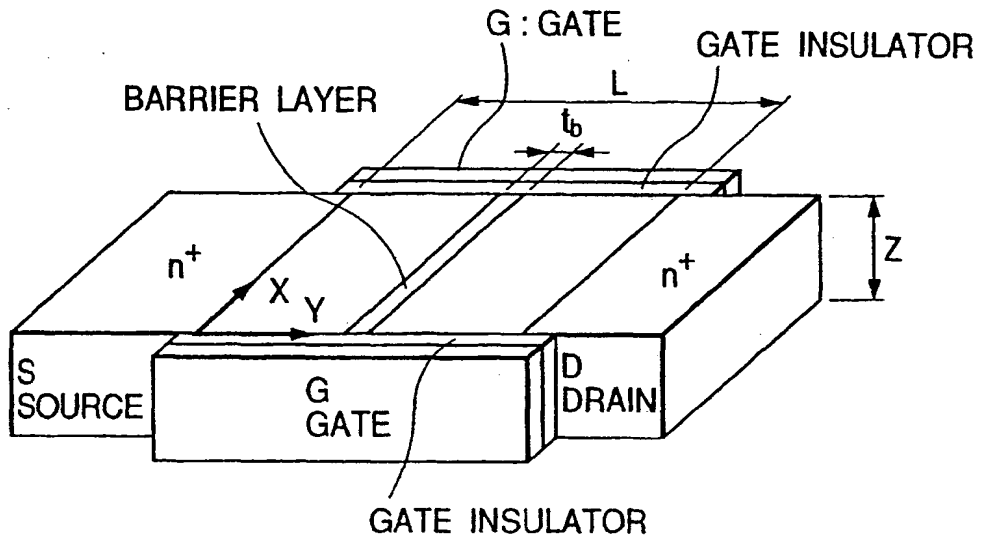


FIG. 9

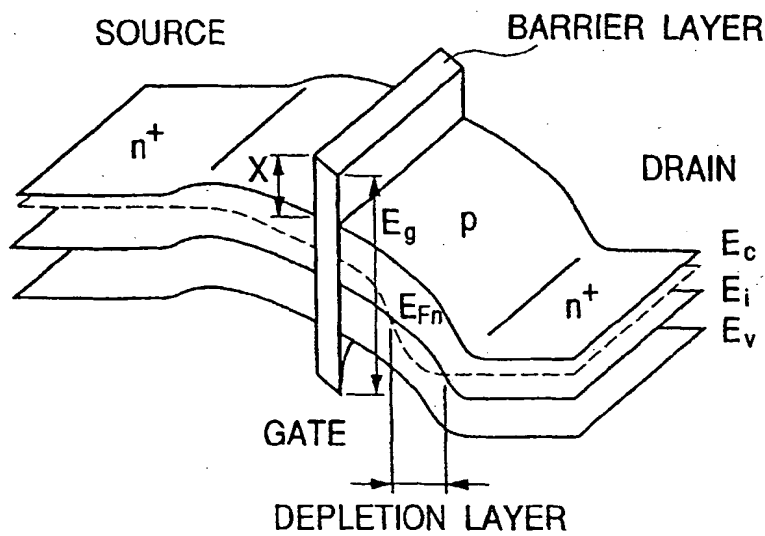


FIG. 10

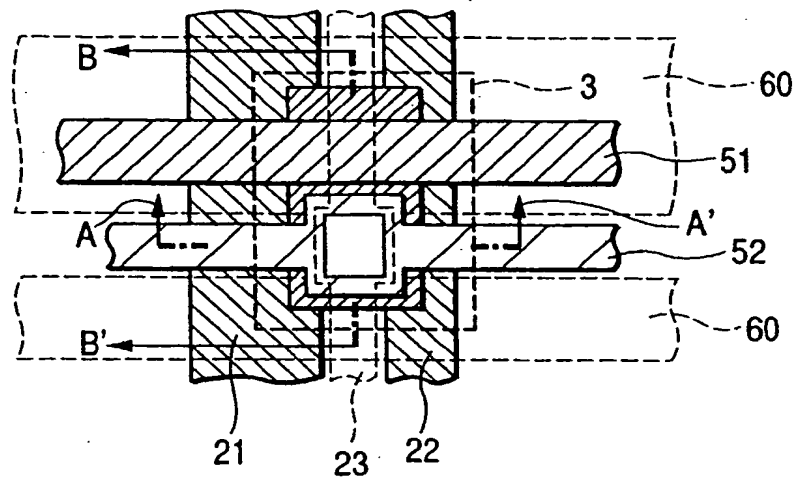


FIG. 11

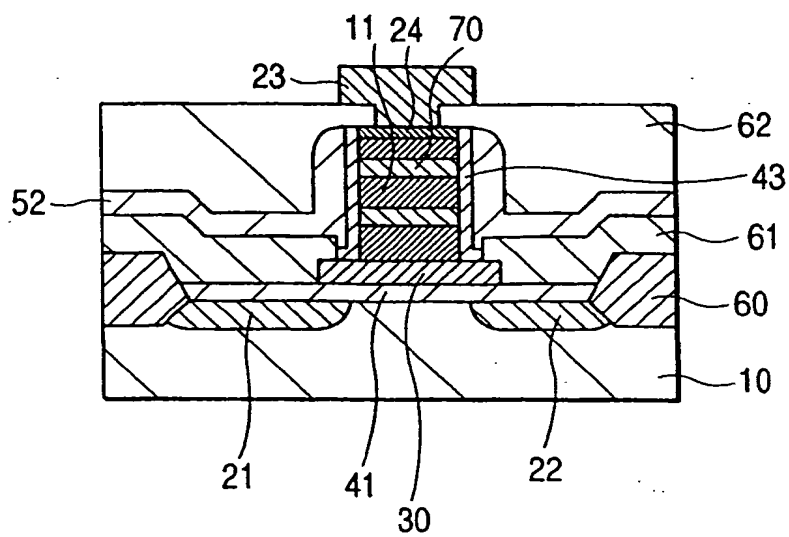


FIG. 12

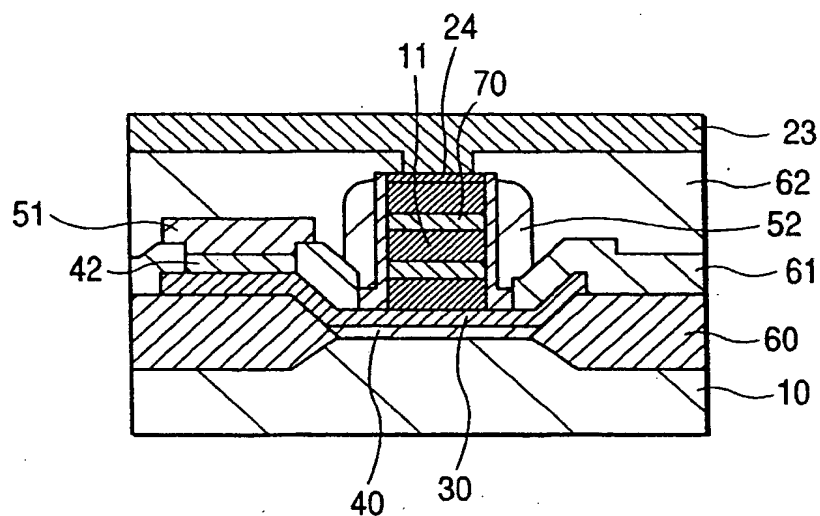


FIG. 13

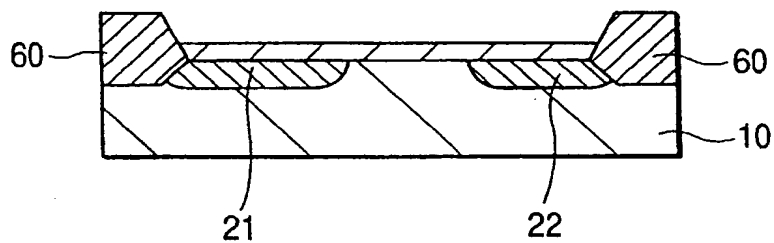


FIG. 14

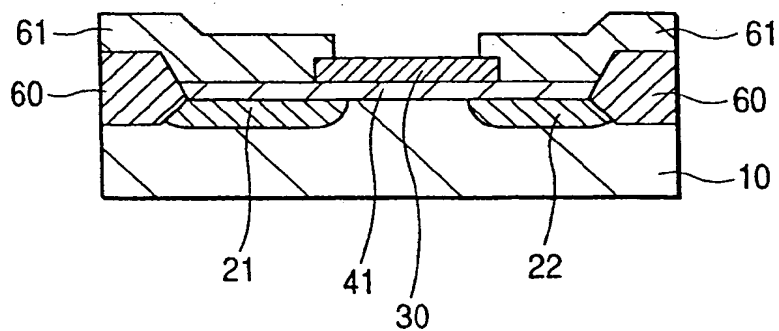


FIG. 15

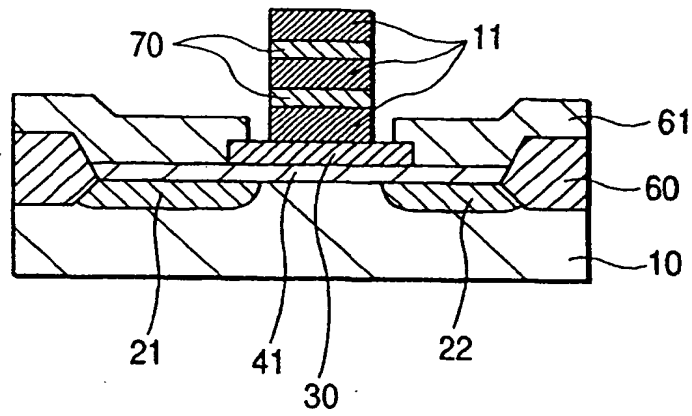


FIG. 16

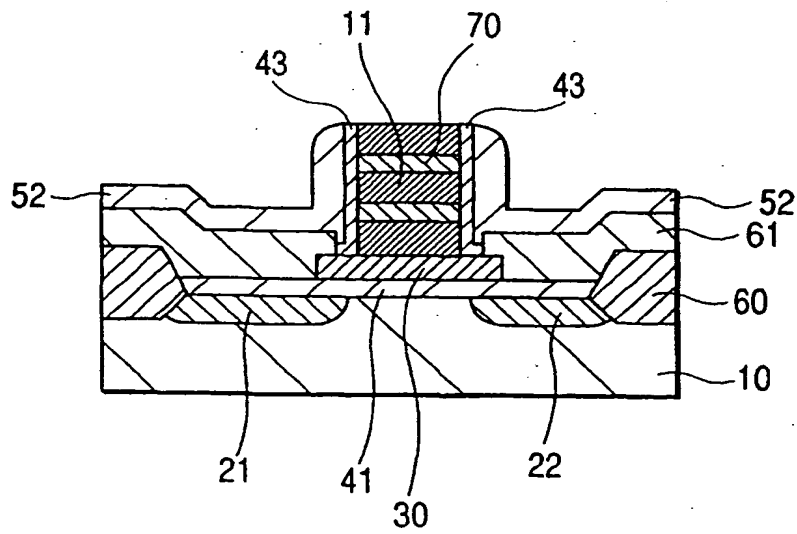
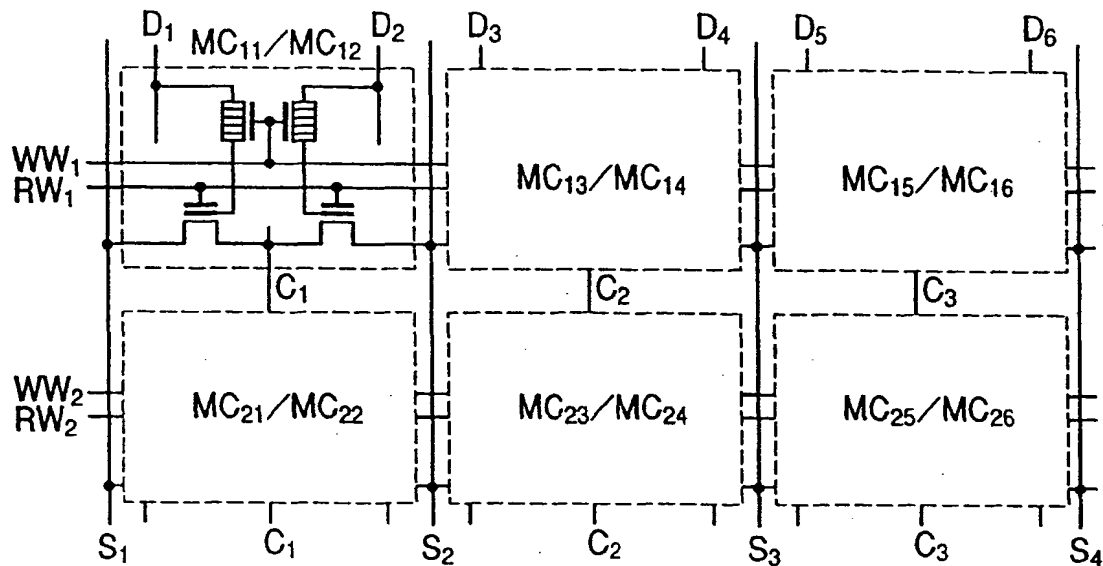


FIG. 17

$S_1 - S_4$: SENSE LINE
 $C_1 - C_3$: CONTROL LINE
 $D_1 - D_6$: DATA LINE
 RW_1, RW_2 : 1ST WORD LINE
 WW_1, WW_2 : 2ND WORD LINE

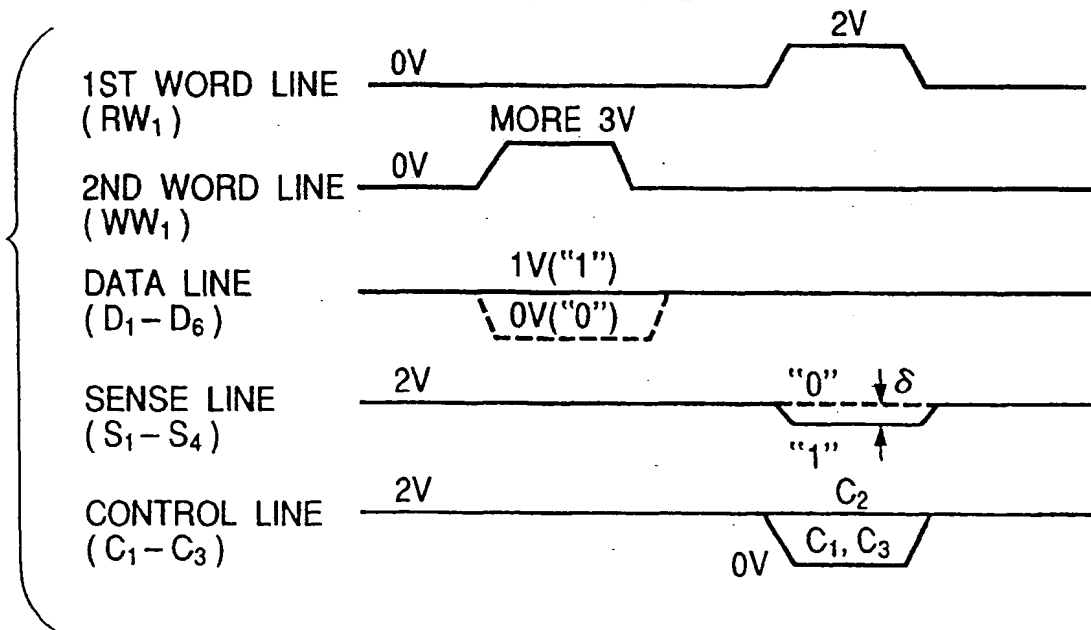
FIG. 18

FIG. 19

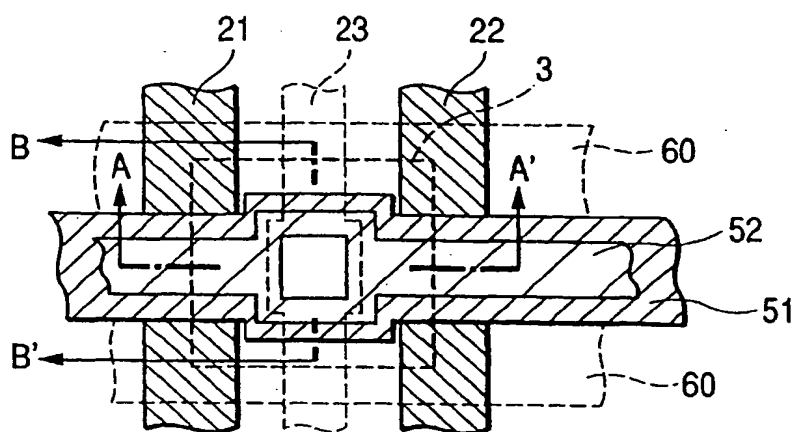


FIG. 20

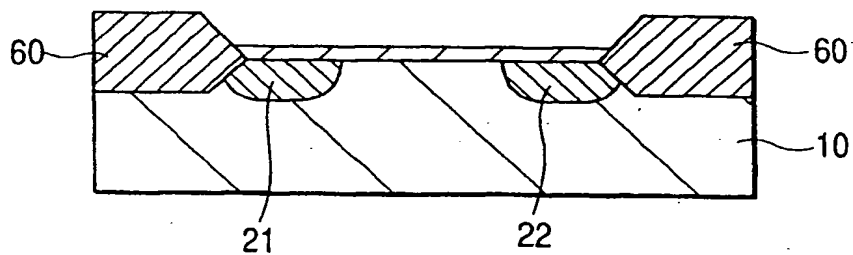


FIG. 21

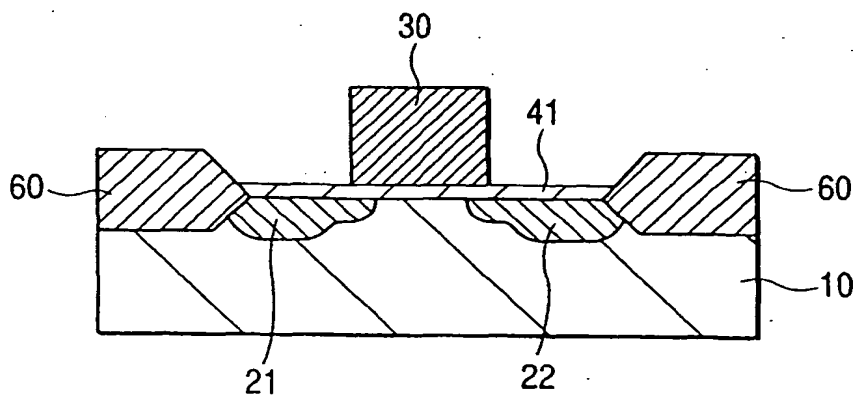


FIG. 22

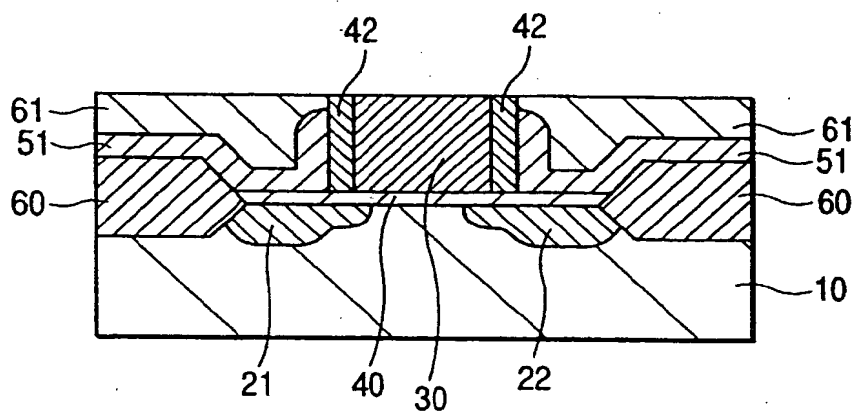


FIG. 23

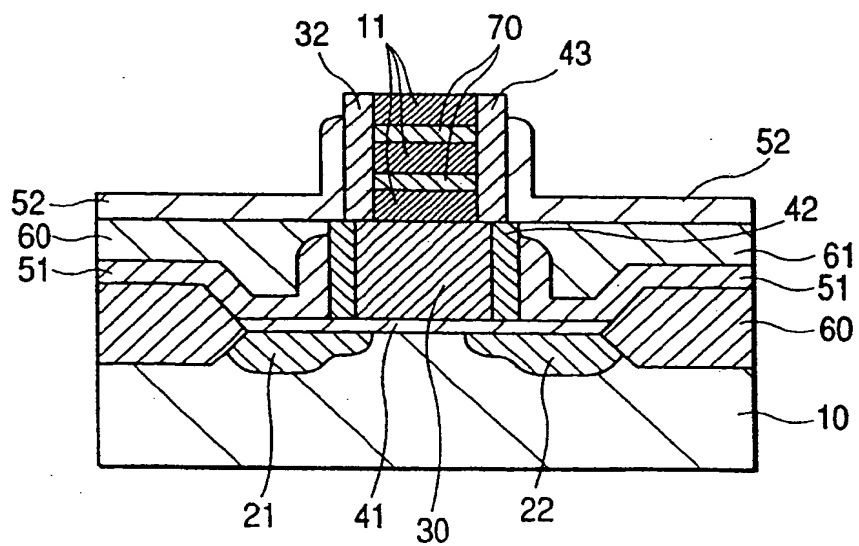


FIG. 24

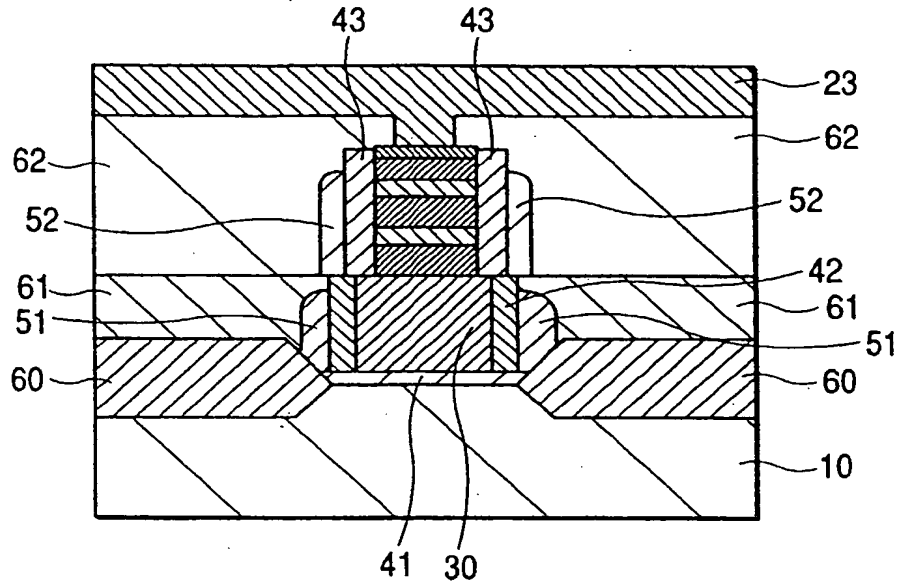


FIG. 25

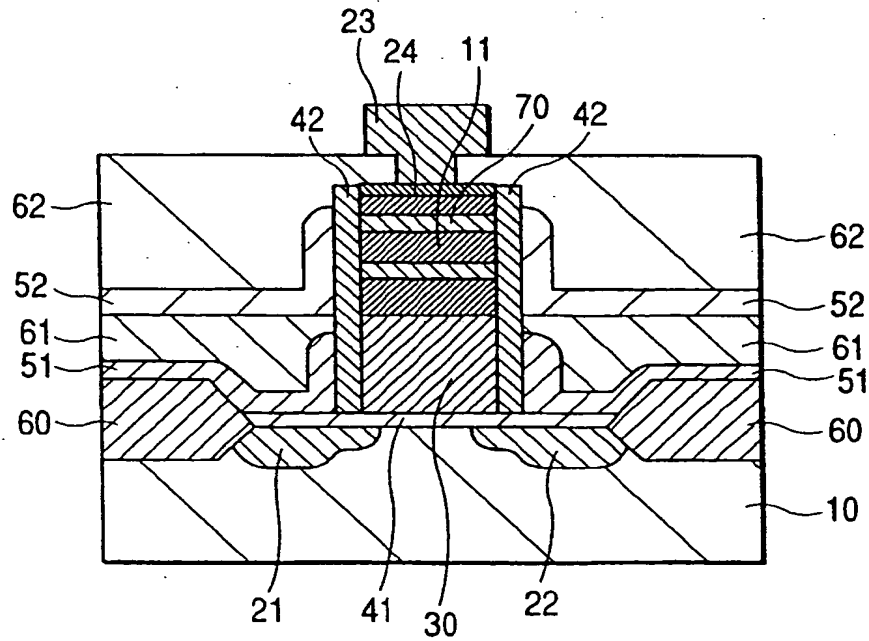


FIG. 26

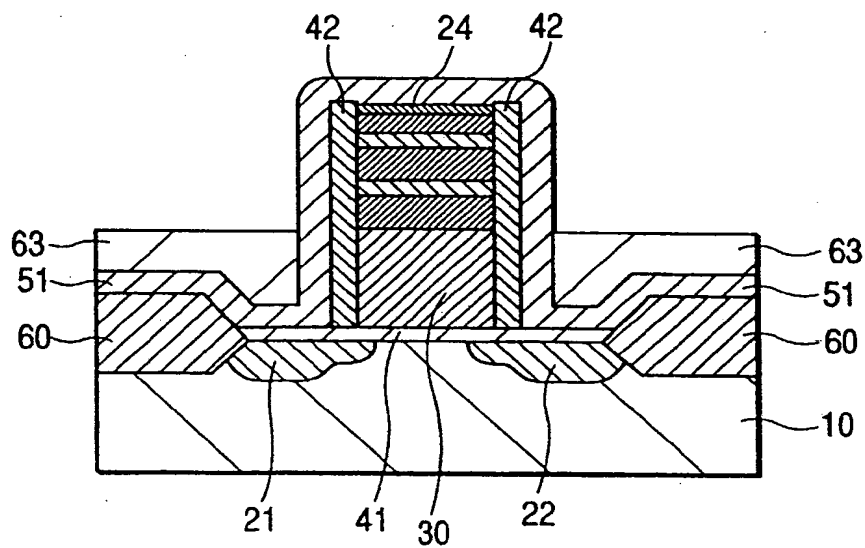


FIG. 27

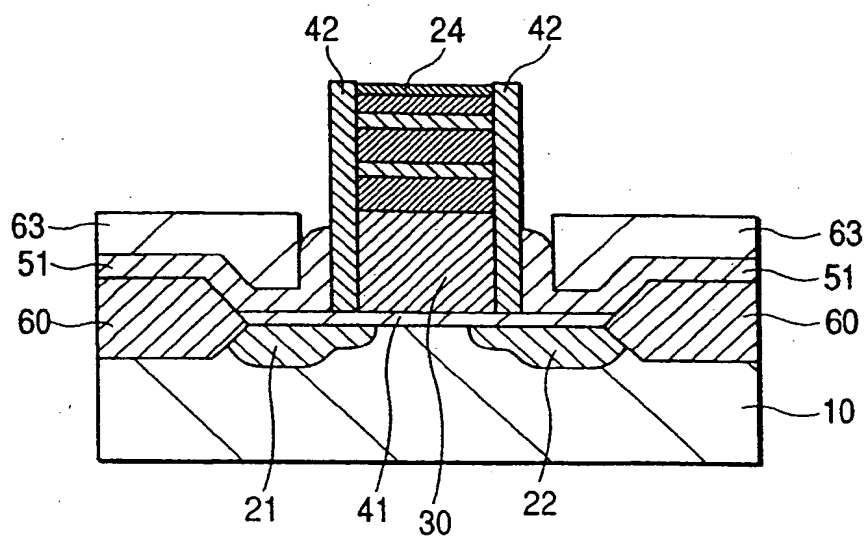


FIG. 28

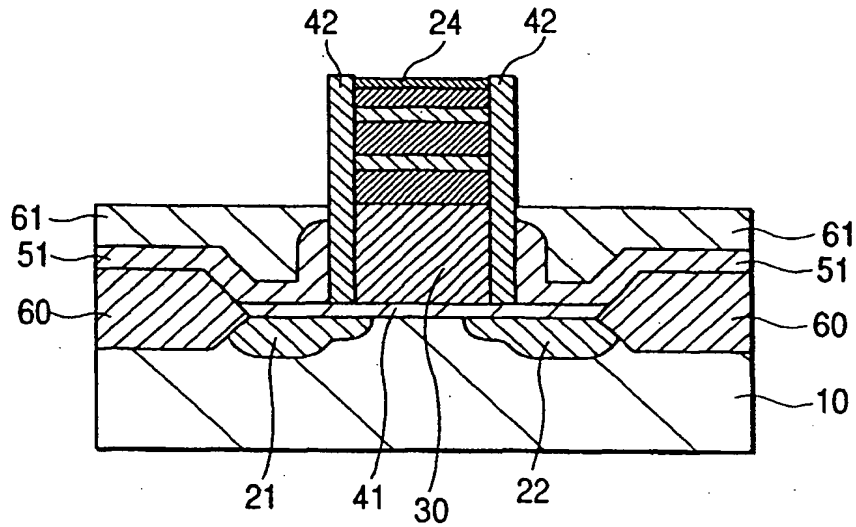


FIG. 29

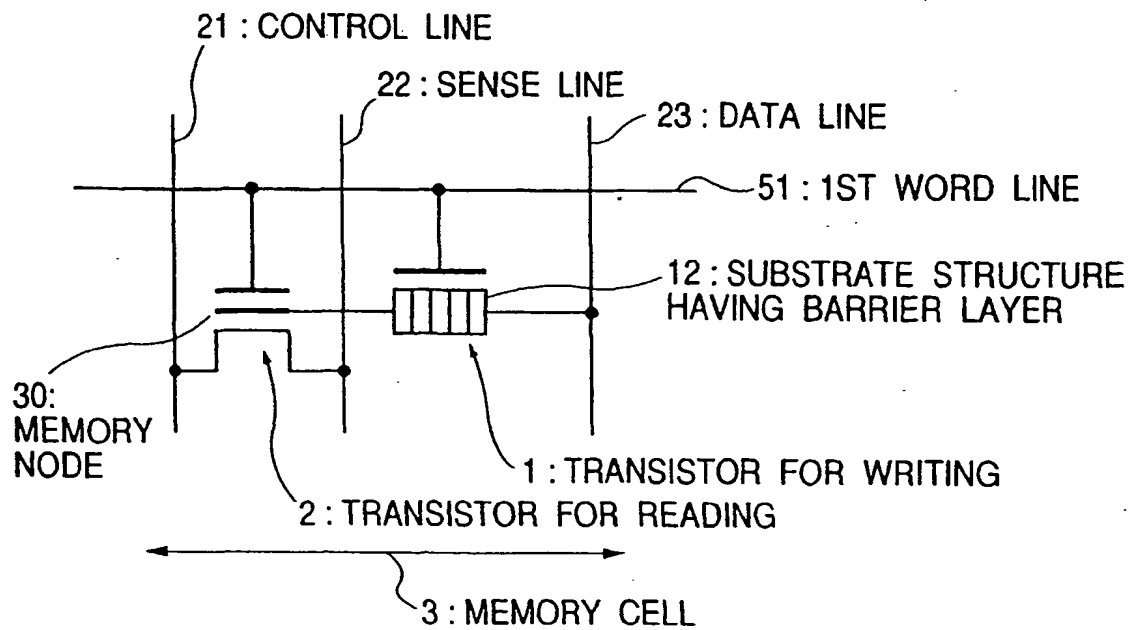


FIG. 30

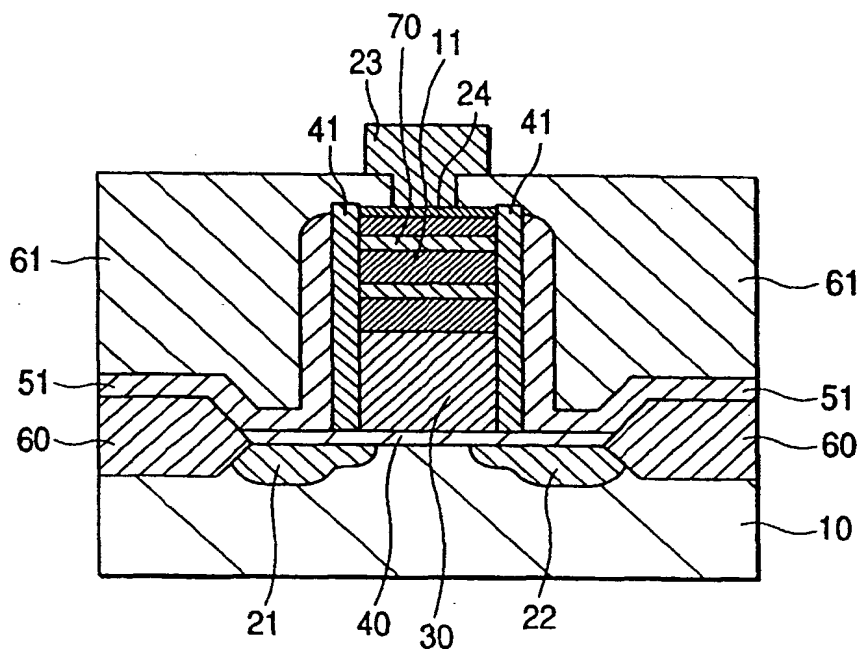


FIG. 31

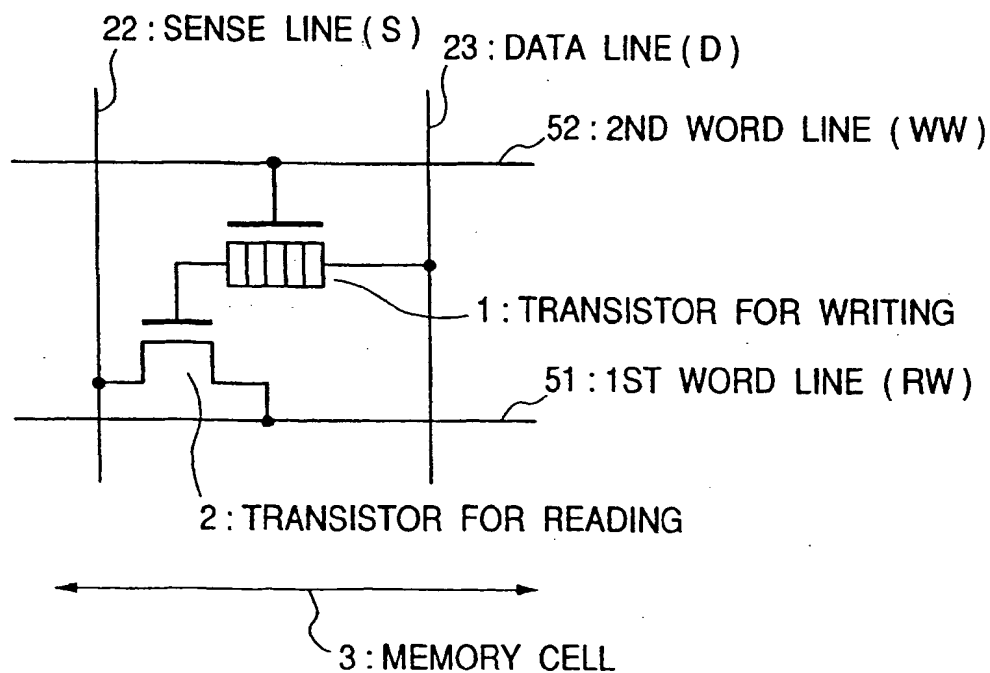
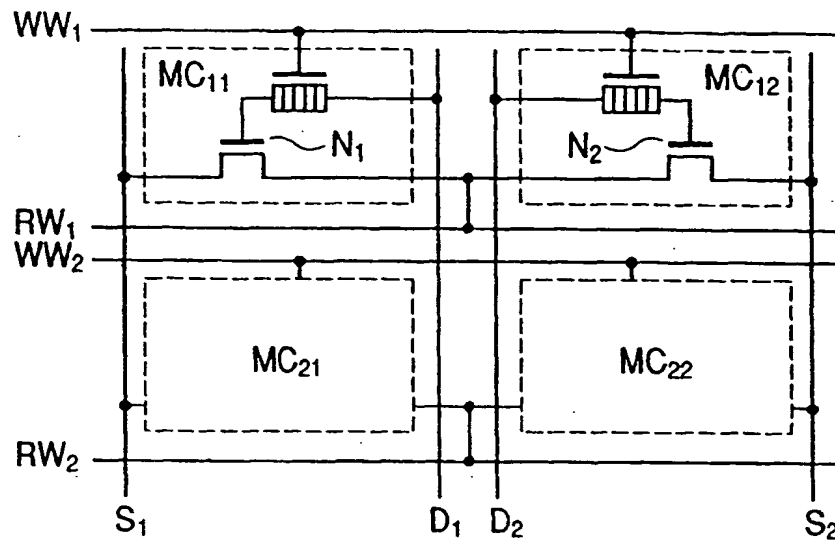


FIG. 32



S_1, S_2 : SENSE LINE
 D_1, D_2 : DATA LINE
 N_1, N_2 : MEMORY NODE
 RW_1, RW_2 : 1ST WORD LINE
 WW_1, WW_2 : 2ND WORD LINE

FIG. 33

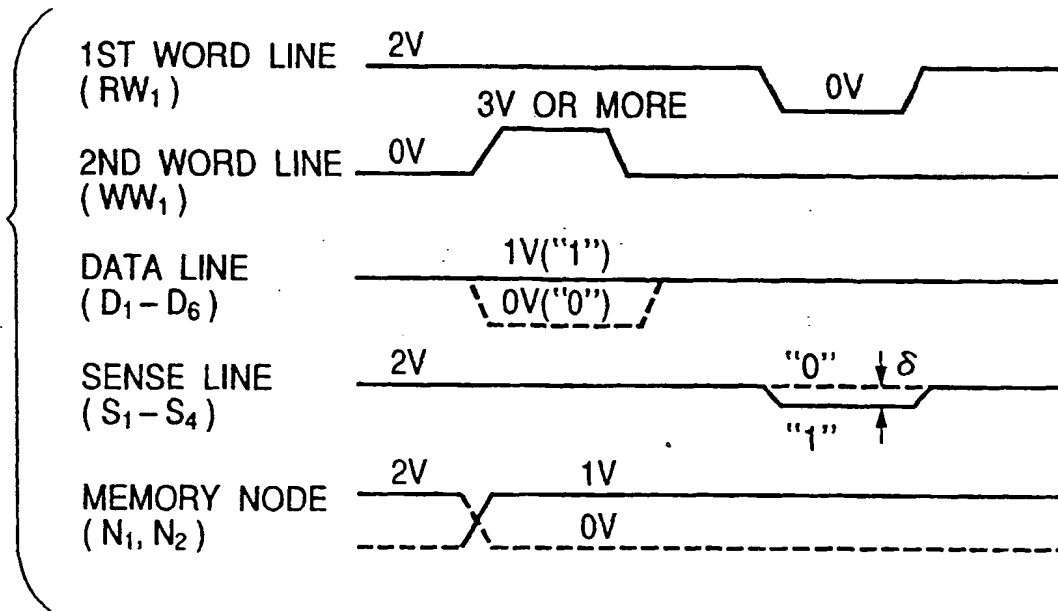


FIG. 34

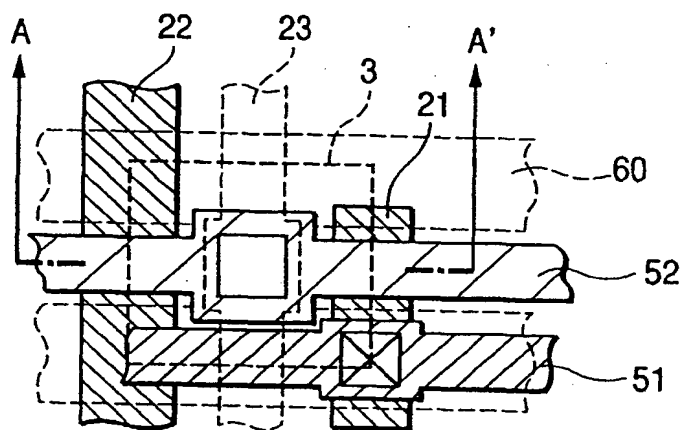


FIG. 35

